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FILING DATE: ***September 16, 2003***

By Authority of the
COMMISSIONER OF PATENTS AND TRADEMARKS

N. WILLIAMS
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No.

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☐ *Additional inventors are being named on the_____ separately numbered sheets attached hereto*

TITLE OF THE INVENTION (500 characters max)

Electric Ultimate Defects Analyzer Detecting all Defects in PCB

Direct all correspondence to: **CORRESPONDENCE ADDRESS**

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ENCLOSED APPLICATION PARTS *(check all that apply)*

☒ Specification *Number of Pages* 7 ☐ CD(S), Number

☒ Drawing(s) *Number of sheets* 4 ☐ Other (specify)

☐ Application Data Sheet. See 37 CFR 1.76

METHOD OF PAYMENT OF FILING FEEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☒ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check or money order is enclosed to cover the filing fees

☐ The Commissioner is herby authorized to charge filing fees or credit any payment to Deposit Account Number:

☒ Payment by credit card. Form PTO-2038 is attached.

FILING FEE AMOUNT($)

$80

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☐ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are:_____

Respectfully submitted,

SIGNATURE _____ Date 09/09/03

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USE ONLY FOR FILING A PRVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is used by the public to file (and by the PTO to process) a Provisional application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to Complete, including gathering, preparing, and submitting the complete provisional application to the PTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETE FORMS TO THIS ADDRESS. SEND TO: Box Provisional Application, Assistant Commissioner for Patents, Washington, D.C. 20231.

Electric ultimate Defects Analyzer detecting all defects in PCB

ABSTRACT

A system for electric testing PCB/MCM before and after assembly. The system uses energy taken from a heating source, timely applied at certain ports of the PCB (entry ports). The energy is defused through the board inner layer tracks terminating at the end of the channel tracks of the PCB (exit ports). The rate of energy diffusion on the board is measured at the terminating ports in the time domain. Measurements can be taken as discrete measurements or as integrated measurements. The measurements results are compared with the pre-memorized values of a group of patterns that represent respective prefect board. Defect analysis is automatically achieved based on learned defect test patterns.

BACKGROUND

The present invention relates to the field of PCB/MCM testing technologies and methods following bare PCB/MCM production process as well as assembled boards/MCM base material. More precisely it is a PCB defect detection system using thermal diffusion technology.

At present, there are two major methods for electrically testing printed circuit boards (PCB), the traditional bed of nails method and the flying probe method. The bed of nails is a resistance measurements method comprised of springy pins

which are electrically connected to pads on the PCB. During the test signals are applied to some of the nails, and measurements are taken at other nails. The bed of nails device needs to be especially designed, built and programmed to fit the structure of the tested PCB type. Each PCB needs a different device.

The flying probe method is based on moving probe(s) physically from one point to another, touching the board and conducting the same tests made by the bed of nails but sequentially. This method eliminates the need to build the physical element required by the bed of nails method, but it still requires making physical contact with the board while conducting electrical tests. Bed of nail tests is limited to a minimum pitch size of 600 micrometer. The method of testing PCBS by flying probe is limited to a minimum pitch size of 300 micrometer. For bed of nail the test time can take between 1 and 2 minutes per PCB, for flying probes the test time is more than two hours. There is therefore a need for a PCB testing method which does not require making physical contact with the board, thus decreasing the pitch size limit and decreasing the testing time considerably and improving the tests' reliability.

THE OBJECT OF THE INVENTION

The object of the invention is to build a PCB/MCM electric test system that will not require any physical contact between the testing device and the board. This method will significantly increase the speed of testing (hundred time and more), will enable testing 5 micron pitch complicated boards and will significantly increase the reliability of the test . The system can test continuity, trace

resistance, detect current leakage, impedance control and perform tests that will represent high voltage tests.

BRIEF DESCRIPTION OF THE DRAWINGS

These and further features and advantages of the invention will become more clearly understood in the light of the ensuing description of a preferred embodiment thereof, given by way of example only, with reference to the accompanying drawings, wherein-

Fig 1 illustrates the typical defects detection analysis methods

Fig 2 illustrates several examples for different kinds of PCB defects

Fig 3 illustrates three dimensional presentation of the PCB defects.

Fig 4 is the system's block diagram

DESCRIPTION

1. TEST METHODE

The entrance ports of the PCB tracks are illuminated, causing heat transfer along the tracks. The entrance ports are beamed selectively or mutually by a regular light source or a laser beam. The temperature rise at the entrance

ports is affected by the illumination duration, in compliance with the PCB's material specifications. PCB tracks are made of copper with some degree of contamination. As a result of the heating process at the entrance ports, a heat wave propagates along the track. The heat is diffused along the tracks and the exit ports. For analyzing the diffusion at the exit port of the track, the respective diffusion equation for the specific material is applied using the respective diffusion coefficient. The rate of diffusion along the tracks depends on the diffusion coefficient. This coefficient value for the specific material is proportional to the conduction coefficient, and inverse-proportion to the density of the material and the heat intensity. This coefficient value is also a function of the initial conditions (rate of change of temperature at the entrance ports).

The results of rise in temperature at exit port/s, occur in time delay with respect to temperature rise at the entrance port. The temperature measurement with respect to time at the exit port/s is a crucial parameter for the analysis. The radiant flux emitted from the exit port is wavelength dependent and proportional to the emissivity of the specific copper track. Emissivity of metals is proportional to their density and inverse-proportion to their temperature. The analysis of the exit ports can be preformed either by using an infrared spectrometer or a thermal imaging apparatus. The measurements are taken with respect to a time domain wavelength or with respect to an integration of the whole spectral emittance. Any existing defect along the track will affect the heat diffusion along the track and cause time

domain changes in thermal characteristics at the exit port. During the manufacturing process of the device, it is initially calibrated both for defect free tracks and for tracks which exceeds determined tolerance (as defined by the net-list IPC-D350/356). The data obtained from the calibration process is used as reference for detecting defects on the board.

2. HEATING SOURCES

The heating source apparatus may be a xenon flash lamp, incandescent lamp, laser, LED, arc lamps or any other light source that fits the testing requirements. The type of heating source is selected according to the following criteria:

a. The illumination of the tracks entrance ports which is preformed simultaneously or one at a time .

b. The duration of illumination which may vary from few milliseconds to few seconds.

c. The use of collimating optics between the source and the entrance ports.

3. TEST PROCESS WORKFLOW AND ANALYSIS

The testing procedure at the exit ports changes according to the analysis measuring method. It considers any combination of the following:

A. using an infrared spectrometer via collimating optics to analyze the temperature of each exit port with respect to time and wavelength.

B. The same method as in A, but checking a spectral window with respect to time instead of a single wavelength.

C. Using a thermal imaging device to analyze each or all exit ports simultaneously. Test results of the exit ports are compared to a database of an identical perfect track.

"Thermal pictures" is a known technology in the context of software for picture analysis. The present invention is based on thermal conduction of copper made tracks and the analysis of the temperature through the infrared emittance at the edges (exit ports of the tracks). Defects along the tracks will affect the heat conduction and therefore will change the thermal picture at the exit port. These defects ultimately change the spectral emittance at the exit ports. The analysis of the spectrum with respect to time enables spotting those defects and their severity.

While the above description contains many specifications, these should not be construed as limitations on the scope of the invention, but rather as exemplifications of the preferred embodiments. Those skilled in the art will envision other possible variations that are within its scope. Accordingly, the scope of the invention should be determined not by the embodiment illustrated, but by the appended claims and their legal equivalents.

What is claimed is:

1. A method for testing PCB/MCM before and after assembly, by checking energy diffusion through boards tracks, said method comprising the steps of:

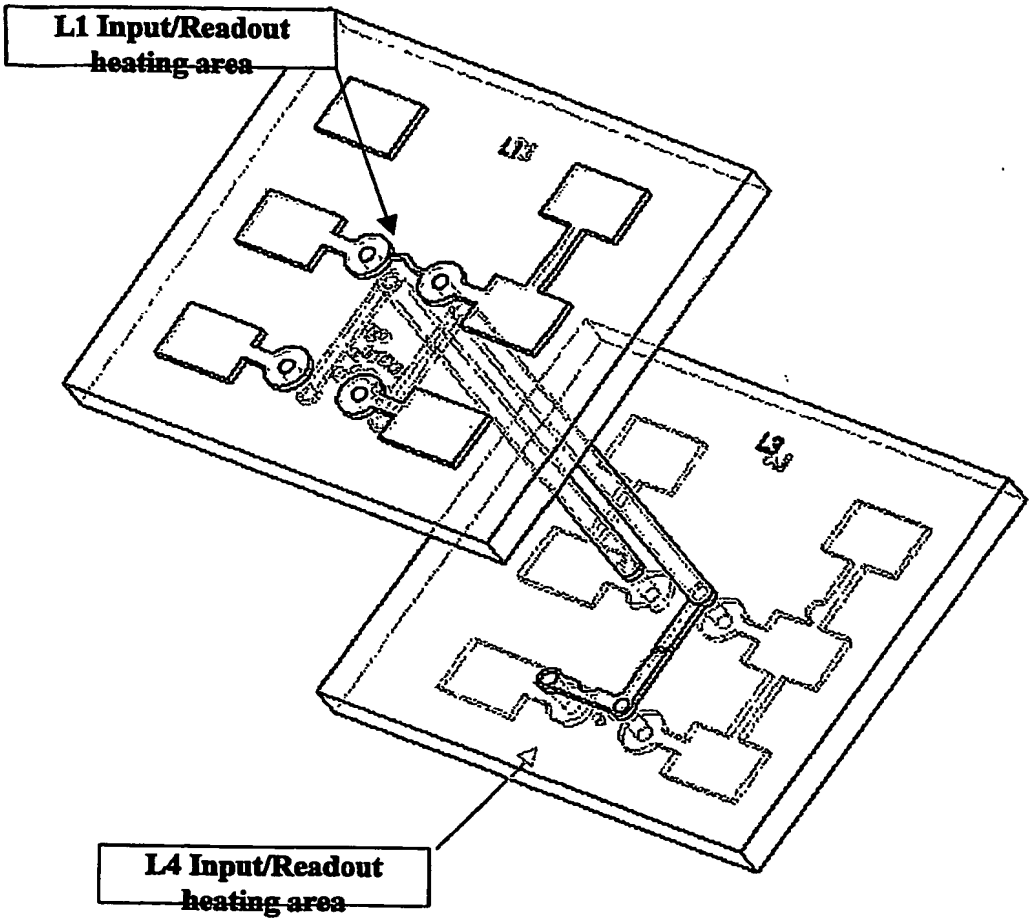
   A. Applying heat energy at certain ports of the PCB (entry ports).

   B. measuring in time domain (discrete or integrated measurements) the rate of energy diffusion along the tracks of the board at terminating ports.

   C. Comparing said measurements with pre-memorized values of a group of patterns that represent respective perfect board results.

   D. Analyzing defects automatically on the basis of learned defect test patterns.

Figure 1: Typical defects detection methods and analysis

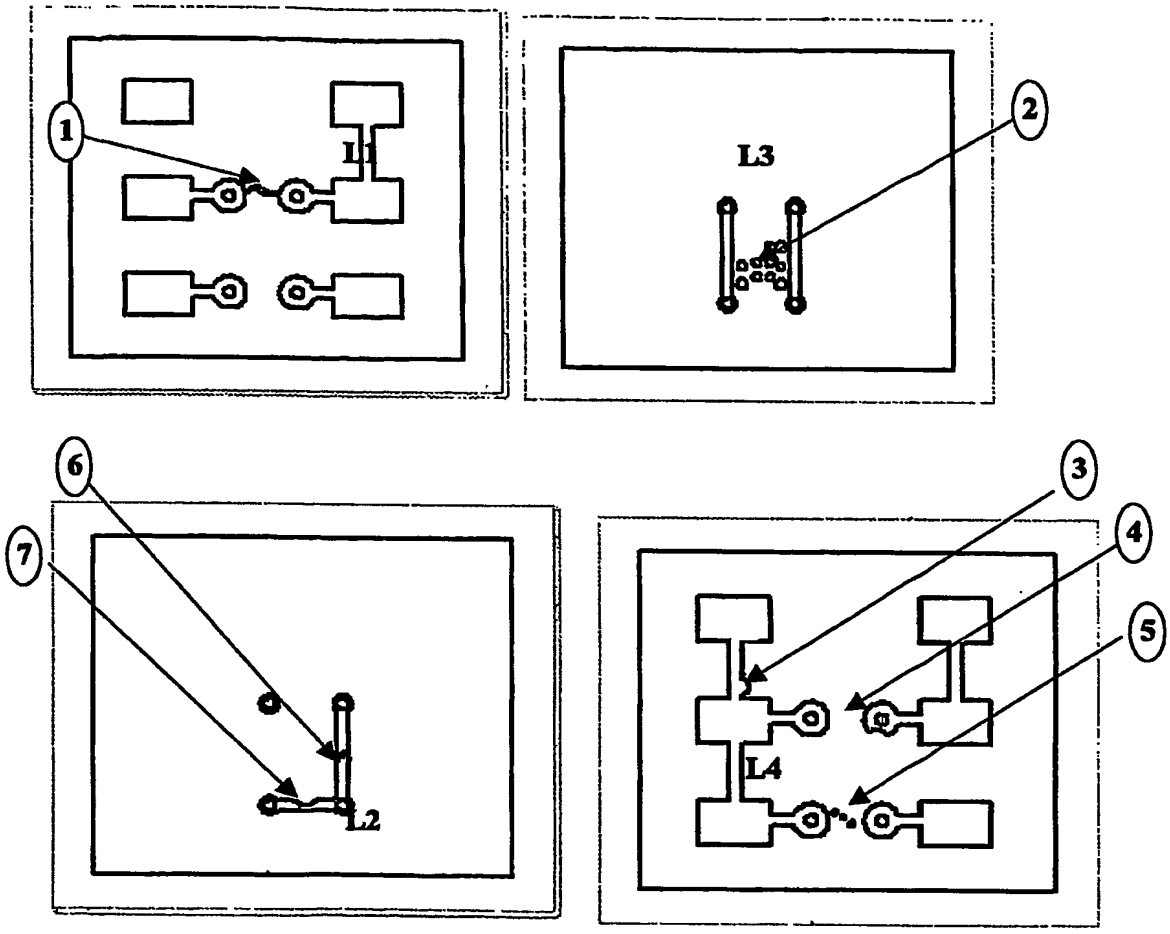


Upper (L1) and lower (L4) layer can be equally treated as input or readout layer, individually or simultaneously.

Our checking method can detect the following electrical phenomena:

- **Irregular impedance**
- **Current leakage**
- **Voltage breakthrough**
- **Continuity test: Sh rten / Op n**
- **Resistance – ut f range** (does not comply with manufacture specification), **betwe n traces r layers, b tween planes as w ll.**

Figure 2: Defects examples



B l w are the descriptions of each defect method:

D f ct #1: Shortage between channels

D f ct #2: Current leakage between channels & low resistance (caused by islands)

D f ct #3: High resistance (caused by thick copper conductor)

D f ct #4: Low resistance (caused by 'eaten' via)

D f ct #5: Breakthrough / leakage (caused by islands between pads)

D f ct #6: Open channel (caused by etching malfunction due to unclear photo resist - *Reston*)

D f ct #7: Low resistance (caused by etching malfunction due to unclear photo resist - *Reston*)

Figure 3

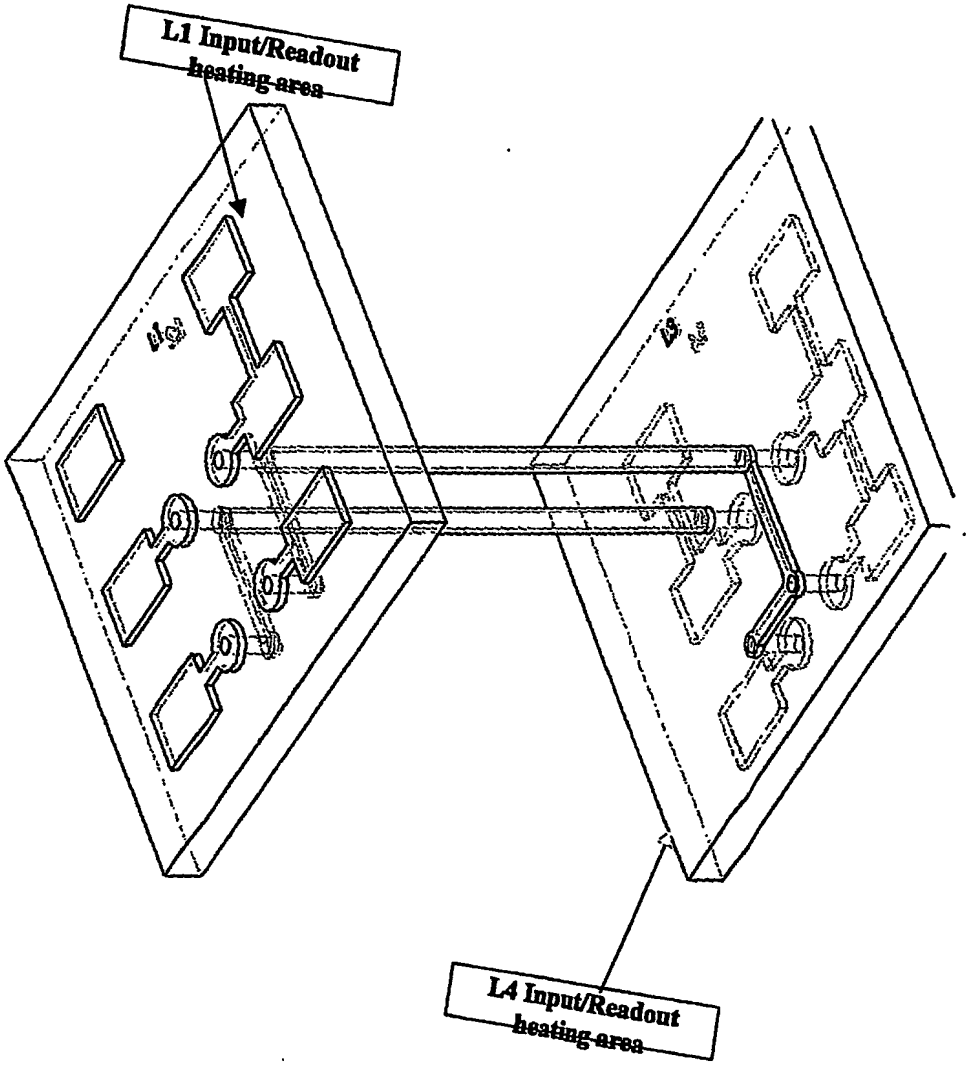
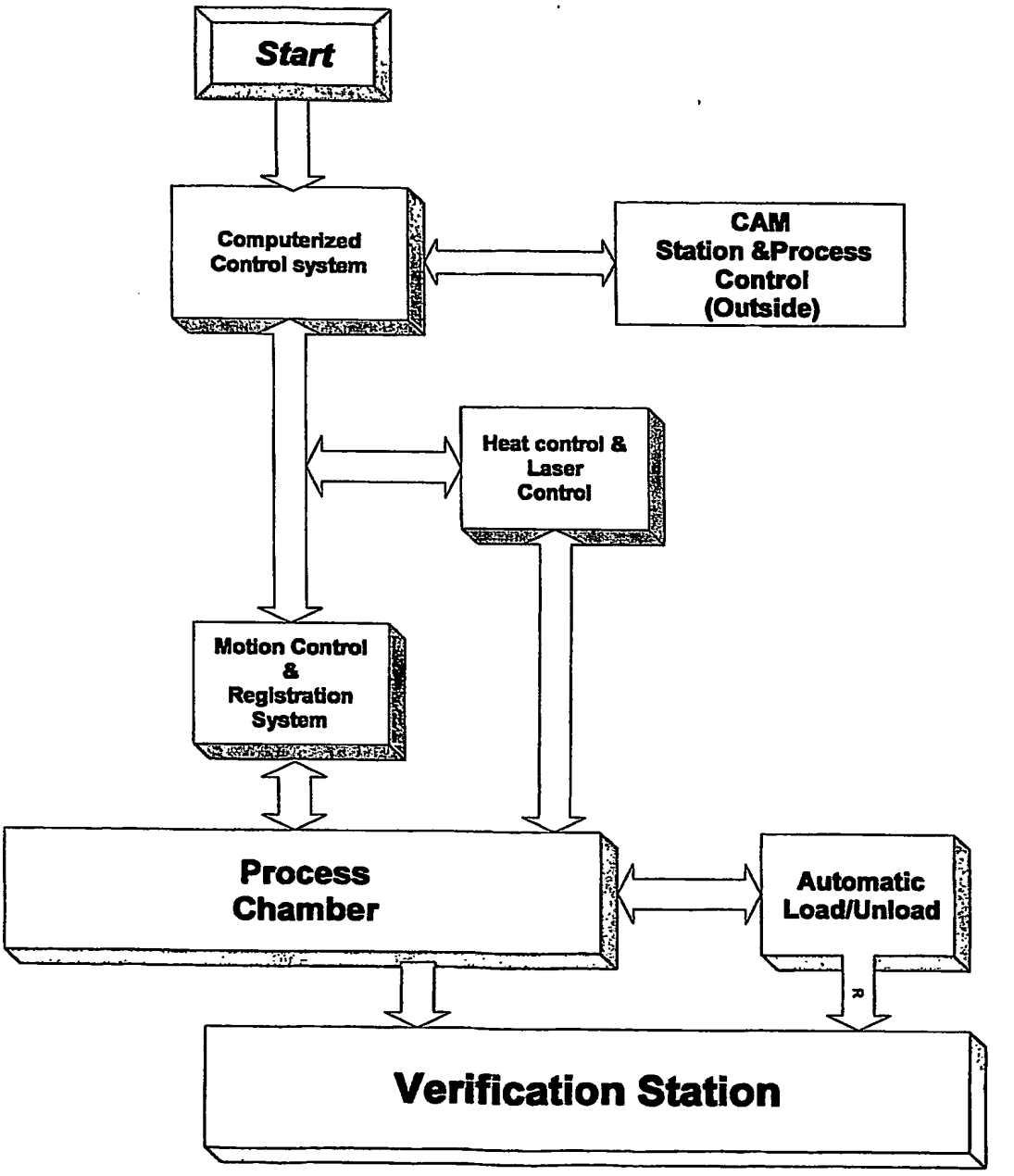

L1 Input/Readout heating area
L4 Input/Readout heating area

Figure 4:


Start
Computerized Control system
CAM Station &Process Control (Outside)
Heat control & Laser Control
Motion Control & Registration System
Process Chamber
Automatic Load/Unload
R
Verification Station

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